Course Syllabus
Gyanmanjari College of Computer Application
Semester-2(BCA)

Subject: Digital Computer Organization - BCAXX12306

Type of course: Minor Stream

Prerequisite: Basic knowledge of Computer

Rationale:

This course provides detail of computer system's functional components, their characteristics, performance and interactions including logical gates, digital logical circuits, arithmetic circuits, system bus, and different types of memory unit and Instruction& Execution of CPU. This course also covers the architectural issues such as instruction set program and data types. On top that, the students are also introduced to the increasingly important area of parallel organization. This course also serves as a basic to develop hardware related projects. And hence it is an important course for all students of computer application.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks					Total Marks
				SEE		CCE			
CI	T	P	C	Theory	Practical	MSE	LWA	ALA	
3	0	2	4	75	25	30	20	50	200

Legends: CI-Class Room Instructions; T – Tutorial; P - Practical; C – Credit; SEE - Semester End Evaluation; MSE-Mid Semester Examination; LWA – Lab Work Assessment; V– Viva voce; CCE-Continuous and Comprehensive Evaluation; ALA-Active Learning Activities.

3Credits * 25Marks =75Marks (each credit carries25 Marks) Theory
1Credits*25 Marks=25Marks (each credit carries 25 Marks) Practical
SEE 100 Marks will be converted into 50 Marks
CCE 100 Marks will be converted into 50 Marks
It is compulsory to pass in each individual component.

Course Content:

Sr. No	Course content	Hrs.	% Weightage
1	**Gates & Boolean Algebra** Introduction to gates and invertors Boolean algebra with truth table Preparing truth table for given circuit Preparing truth table for given circuit (SOP&POS) De Morgan's theorem	12	25%
2	**Basic digital logical circuits** Integrated circuits Encoder, Decoder, Multiplexer, Demultiplexer, Comparators	10	25%
3	**Arithmetic circuits** Shifters Adders, Subtractors, Half adder, Full adder Binary adder/subtractors	08	20%
4	**Memory units** Latches (RS, D, level locking) Flip-flops (SR,D, JK) Registers (shift, buffer, controlled) Counters – Synchronous & Asynchronous Counters, Ripple Counter, Counters with Increment & Decrement Facility, Computer bus, Bus width, bus clocking, arbitration, operations	08	15%
5	**Instructions and Execution** Instruction Execution, Parallel Instruction Execution, CPU organization. RISC versus CISC, Instruction Level Parallelism, Processor Level Parallelism, Instruction formats - Types of Instruction, Types of operand Addressing modes	07	15%

Continuous Assessment:

Sr. No	Active Learning Activities	Marks
1	**Logic Gate Challenges:** Set of challenges assign to the student to prepare logic gates circuits in order to produce the desired output for the given inputs. Student have to upload the solved challenges on GMIU Web Portal.	10
2	**Logical Circuit on Canvas:** Student will create digital logical circuit (using different kinds of gate) on given topic and upload it on GMIU Web Portal.	10
3	**Circuit Dilemma:** Circuit Dilemma is scenario-based questions to evaluate student on their ability to solve problems using logic and analytical thinking. It will be taken on GMIU Web Portal.	10
4	**Circuit Simulator:** Student will build and simulate circuit's on given definition in group of 4 student. Student have to upload the solved definition on GMIU Web Portal.	10
5	**Attendance**	10
Total		50

Suggested Specification table with Marks (Theory):75

Distribution of Theory Marks (Revised Bloom's Taxonomy)						
Level	Remembrance (R)	Understanding (U)	Application (A)	Analyze (N)	Evaluate (E)	Create (C)
Weightage	25 %	45 %	10 %	10 %	10 %	00 %

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

Course Outcome:

After learning the course, the students should be able to:	
CO1	Identify and explain the basic structure and functional units of a digital computer.
CO2	Analyze & design the digital logical circuit.
CO3	Understand the memory unit of computer system.
CO4	Understand and design the arithmetic circuits.

CO5	Relate design principles in instruction set design including RISC & CISC architectures.

List of Practical

Sr. No.	Descriptions	Unit No.	Hrs
1	Identify various ICs and their specification a. OR gate b. AND gate c. NAND gate d. NOR gate	1	4
2	To realize why NAND gate is known as the universal gate by implementation of: a. NOT using NAND b. AND using NAND c. OR using NAND d. XOR using NAND	1	4
3	Implementation of the given Boolean function using logic gates in both SOP and POS forms.	1	2
4	a. To design and setup a 4:1 Multiplexer (MUX) using only NAND gates. b. To design and setup a 1:4Demultiplexer (DE-MUX) using only NAND gates.	2	4
5	Implementation of 4x1 multiplexer using logic gates.	2	2
6	To realize a. Half Adder and Full Adder b. Half Subtractor and Full Subtractor by using Basic gates and NAND gates.	3	2
7	Implementationof4-bitparalleladderusing7483IC.	3	2
8	a. Truth Table verification of 1) RS Flip Flop 2) T type Flip Flop. 3) D type Flip Flop. 4) JK Flip Flop. b. Conversion of one type of Flip flop to another	4	6
9	Design, andverifythe4-bitsynchronouscounter.	4	2
10	Design and verify the 4-bit asynchronous counter.	4	2
		Total	30

Instructional Method:

The course delivery method will depend upon the requirement of content and need of students. The teacher in addition to conventional teaching method by black board, may also use any of tools such as demonstration, role play, Quiz, brainstorming, MOOCs etc.

From the content 10% topics are suggested for flipped mode instruction. Students will use supplementary resource such as online videos, NPTEL/SWAYAM videos, e-courses, Virtual Laboratory.

The internal evaluation will be done on the basis of Active Learning Assignment.

Practical/Viva examination will be conducted at the end of semester for evaluation of performance of students in laboratory.

Reference Books:

[1] Tanenbaum A. S.: Structured Computer Organization, Prentice – Hall of India Pvt. Ltd.
[2] V. Raja Raman: Fundamentals of Computers
[3] Malvino A.P.: Digital Computer Electronics, Tata McGraw, Hill Pub. Co. Ltd.
[4] Thomas Bartee: Computer Architecture & Logic Design, Tata McGraw, Hill Pub. Co. Ltd.
[5] Pal Chaudhuri: Computer Organization and Design, Prentice – Hall of India Pvt. Ltd.