Gyanmanjari Innovative University

Course Syllabus
Gyanmanjari Institute of Technology
Semester-3

**Subject**: Digital System Design - BETEC13301

**Type of course**:Professional Core and Professional Elective Courses

**Prerequisite**: Understanding of Basic Electronics and Digital.

**Rationale:**

This course has been designed to impart in-depth knowledge of Digital System Design .Digital system Design is used in the Electronics industry especially in the VLSI field.. The students learn basic concepts of digital system Design. They will also acquire the knowledge of its applications. In this course students learn about processes like design activities that involve creating visual content for both digital and physical mediums.Field of Digital System Design lies in its fundamental importance in various areas including engineering. technology, and everyday life .

**Teaching and Examination Scheme:**

| Teaching Scheme | | | Credits | Examination Marks | | | | | Total Marks |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Theory Marks | | Practical Marks | | CA | |
| CI | T | P | C | ESE | MSE | V | P | ALA | |
| 4 | 0 | 2 | 5 | 60 | 30 | 10 | 20 | 30 | 150 |

*Legends: CI-Classroom Instructions; T – Tutorial; P - Practical; C – Credit; ESE - End Semester Examination; MSE- Mid Semester Examination; V – Viva; CA - Continuous Assessment; ALA- Active Learning Activities.*

**Course Content:**

| Unit No | Course content | Hrs | % Weightage |
|---|---|---|---|
| 1. | **Basics of VHDL**<br>Introduction to VHDL, Basic Terminology:Entity, Architecture. Different type of Modellings: Dataflow Style of Modeling , Behavioral Style of Modeling, Structural Style of Modeling, Mixed Style of Modeling, Configuration Declaration, Package Declaration.Identifiers , Data Objects ,Operators | 15 | 25% |

| | | | |
|---|---|---|---|
| 2. | **Dataflow , Behavioral and Structural Style of Modeling**<br>Dataflow Style of Modeling:Concurrent Signal Assignment Statement, Conditional Signal Assignment Statement, Selected Signal Assignment Statement, Behavioral Style of Modeling - signal, variable, Process Statement, Variable Assignment Statement, Signal Assignment Statement, Wait Statement, If, Case, Loop, Exit, Next Statement, Programming of combinational circuit using Data flow and Behavioral, Structural Style of Modeling, Component Declaration, Component Instantiation, Program based on above. | 21 | 35% |
| 3. | **Finite State Machines**<br>Introduction to FSM,components and Types of FSM(Mealy and Moore machine ,State diagram,programming of Mealy and Moore using Dataflow and Behavioral Style of Modeling. | 12 | 20% |
| 4. | **Memory and Programmable Logic**<br>Random-Access Memory,Read only Memory,Programmable Logic Device PLDs, Programmable Logic Array(PLA), Programmable array Logic (PAL) | 12 | 20% |

## Continuous Assessment:

| Sr. No | Active Learning Activities | Marks |
|---|---|---|
| 1 | **Comparative study**<br>Student have to prepare a comparative analysis of Different types of software tools (likeVHDL,Verilog )used for Hardware Descriptive Language and upload Report on GMIU Web Portal | 10 |
| 2 | **Application of FSM**<br>Students have to design an FSM on VHDL Tool (like vending machine controller, a traffic light sequencer.) Upload Design on GMIU Web Portal | 10 |
| 3 | **Code Rescue**<br>Faculty provides a VHDL code snippet for a circuit (e.g., a counter, a multiplexer, a finite state machine) that has a bug, an inefficiency, or a missing feature.Students analyze the code, identify the issue, and modify the VHDL code to correct it.Upload corrected code on GMIU Web Portal. | 10 |
| Total | | 30 |

**Suggested Specification table with Marks (Theory):60**

| Distribution of Theory Marks **(Revised Bloom's Taxonomy)** | | | | | | |
|---|---|---|---|---|---|---|
| Level | Remembrance (R) | Understanding (U) | Application (A) | Analyze (N) | Evaluate (E) | Create (C) |
| Weightage | 20% | 40% | 30% | 10% | 0 | 0 |

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

## Course Outcome:

| After learning the course the students should be able to: | |
|---|---|
| CO1 | Familiarize with the basics of VHDL. |
| CO2 | Focus on the different type of VHDL Modelling and its Implementation. |
| CO3 | Understand the concept of finite State Machine. |
| CO4 | Design and analyze different type of Memories. |

## List of Practicals:

| Sr. No | Descriptions | Unit No | Hrs |
|---|---|---|---|
| 1 | Study of Statement of different Type of Modelling | 1 | 2 |
| 2 | Implement Logic Gates using VHDL | 2 | 2 |
| 3 | Design VHDL code for Full adder using Dataflow Behavioral and Structural Style of Modeling. | 2 | 2 |
| 4 | Write VHDL code for Mux(1:8) | 2 | 2 |
| 5 | Apply VHDL code to generate Dmux(8:1) | 2 | 2 |
| 6 | Implement T and D-flip-flop using Process statement. | 2 | 2 |
| 7 | Write VHDL program for Comparator and check the Waveform. | 2 | 2 |
| 8 | Implement register and counter using VHDL | 2 | 2 |
| 9 | Design VHDL code for JK Flip flop using Structural Style of Modeling. | 2 | 2 |
| 10 | To develop the VHDL code for 16-to-1 Multiplexer using 4-to-1 Multiplexer using simulation tool | 2 | 2 |
| 11 | To develop the VHDL code for BCD to 7-Segment display using simulation tool | 2 | 2 |
| 12 | Implement Moore Machine using simulation tool | 3 | 2 |
| 13 | Design VHDL code for Sequence detector (101) using Moore state machine | 3 | 2 |
| 14 | Apply VHDL code for Mealy Machine using simulation tool. | 3 | 2 |
| 15 | Study of different types of Memory | 4 | 2 |
| | **TOTAL** | | 30 |

## Instructional Method:

The course delivery method will depend upon the requirement of content and the needs of students. The teacher, in addition to conventional teaching methods by black board, may also use any tools such as demonstration, role play, Quiz, brainstorming, MOOCs etc.

From the content 10% topics are suggested for flipped mode instruction.
Students will use supplementary resources such as online videos, NPTEL/SWAYAM videos, e-courses, Virtual Laboratory

The internal evaluation will be done on the basis of Active Learning Assignment
Practical/Viva examination will be conducted at the end of semester for evaluation of performance of students in the laboratory.

## Reference Books:

[1] Douglas perry , "VHDL Programming By Example", By McGraw-Hill
[2] Charles S. Roth,Lizy Kurian John ," Digital Systems Design Using VHDL", Cengage Learning.
[3] Jayaram Bhasker "A VHDL Primer",P T R Prentice Hall Englewood Cliffs.
[4] Kaur Gagandeep "vHDL:Basics of Programming".