Gyanmanjari Innovative University

Course Syllabus
Gyanmanjari Diploma Engineering College
Semester-1
(Diploma)

Subject: Building Blocks of Digital Systems - DET1EE11201

Type of course: Major (Core)

Prerequisite: Basic understanding of electrical components, circuit fundamentals, logical reasoning, and elementary mathematics.

Rationale: This course develops core digital electronics skills by covering logic gates, number systems, Boolean algebra, and circuit design, equipping students to analyze and design real-world digital systems.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks		Total Marks
CI	T	P	C	SEE	CCE	
4	0	2	5	100	50	150

Legends: CI-Class Room Instructions; T – Tutorial; P - Practical; C – Credit; SEE - Semester End Evaluation; LWA - Lab Work Assessment; V – Viva voce; CCE-Continuous and Comprehensive Evaluation; ALA- Active Learning Activities.

Course Content:

Sr. No	Course Content	Hrs.	% Weightage
1	**Number Systems and Logic Gates** **Topics:** • Binary, Decimal, and Hexadecimal conversions • 1's and 2's complement, Binary addition & subtraction • Logic gates: AND, OR, NOT, NAND, NOR, XOR, XNOR – symbols and truth tables • Universal gates – realization of basic gates using NAND/NOR **Practical:**	T:12 P:06	20%

Sr. No.	Practical Task	Tools Used	Learning Outcome
1	Implement basic gates (AND, OR, NOT) and verify truth tables	Digital Trainer Kit	Learn gate-level circuit wiring

2	Implement NAND, NOR, XOR, and XNOR gates, and verify truth tables	Digital Trainer Kit	Analyze gate behavior across environments
3	Realize AND, OR, NOT using NOR gates (universal gate proof)	Digital Trainer Kit	Demonstrate logical universality
4	Realize AND, OR, NOT using only NAND gates (universal gate proof)	Digital Trainer Kit	Demonstrate logical universality
5	Skill Spark: Build a logic-based system	Breadboard	Apply gate logic in simple applications on the Breadboard.

Evaluation Method

Sr. No.	Evaluation Component	SEE (Marks)	CCE (Marks)	Description
1	Digital Circuit Building	10	–	Build the given digital circuit using basic gates on the trainer kit. Realize the same using universal gates and verify the results.
2	Number System Design	–	10	Design a custom number system based on the given base and demonstrate its conversion logic to decimal.
	Total	10	10	

2	**Boolean Algebra and Simplification** **Topics:** • Boolean algebra: laws, theorems, De Morgan's laws • Canonical forms: SOP (Sum of Products) and POS (Product of Sums)	**T:12** **P:06**	**20%**

- K-map techniques: 2, 3, 4-variable simplification
- Realization of simplified expressions using logic gates

Practical:

Sr. No.	Practical Task	Tools Used	Outcome
1	Verify De Morgan's law	Digital Trainer Kit	Understand De Morgan's validation
2	Simplify given expressions using 2, 3, and 4-variable Karnaugh Maps	Karnaugh Map Solver	Reduce expressions efficiently using visual grouping
3	Implement simplified logic expressions (from K-map) using Logisim	Logisim	Translate simplified logic into working circuits
4	Analysis and Synthesis of Boolean Expressions using Basic Logic Gates	Virtual lab	Simulate and implement Boolean expressions using basic logic gates in a virtual lab.
5	Realize SOP/POS expressions using only NAND/NOR gates	Logisim / IC Trainer Kits	Practice hardware-oriente d implementation

Evaluation Method

Sr. No.	Evaluation Component	SEE (Marks)	CCE (Marks)	Description
1	K-Map Simplification and Circuit Realization	15	–	Simplify a Boolean expression using a K-map. Implement the resulting circuit using basic and universal gates. Generate and verify the truth table.

2	Active Learning Activity (SOP to POS Conversion)	–	10	Convert the given SOP expression to its equivalent POS form and verify the truth table using simulation tools. Submit a photo on the GMIU portal.
	Total	15	10	

3 **Combinational Circuits** — T:12 P:06 — 20%

Topics:

- Adders
- Subtractors
- Code Conversion
- Decoders and Encoders
- Multiplexers

Practical:

Sr. No.	Practical Task	Tools Used	Learning Outcome
1	Design and implement Half Adder and Full Adder	Logic Simulator / Logic Trainer Kit	Understand binary addition using logic gates and implement basic adders
2	Design and implement Half Subtractor and Full Subtractor	Logic Simulator / Logic Trainer Kit	Perform binary subtraction and apply subtractor logic circuit design
3	Implement Binary to Gray and Gray to Binary code conversion circuits	Logic Simulator / Logic Trainer Kit	Understand code conversion techniques and logic implementation
4	Realize and verify 2-to-4 decoder and 4-to-2 encoder circuits	ICs (e.g., 74138, 74147), Breadboard	Develop and test decoding and encoding logic circuits

5	Design and implement a 4-to-1 multiplexer using gates or IC 74153	Digital Trainer Kit / Logic Simulator	Demonstrate data selection using multiplexer circuits

Evaluation Method

Sr. No.	Evaluation Component	SEE (Marks)	CCE (Marks)	Description
1	Combinational Circuit Design	8	–	Design and implement a given combinational circuit equation using Multisim. Verify the circuit behavior using simulation output or truth tables.
2	Circuit Finder	7	–	The output and input are given. Judge and simulate the circuit
3	Active Learning Activity (Code Conversion and Converter Designing)	–	10	Build a code conversion circuit using a simulator and upload it to the GMIU portal.
	Total	15	10	

4	**Sequential Circuits**	T:12 P:06	20%

Topics:

- Flip-Flops
- Registers
- Shift Registers
- Counters

Practical:

Sr. No.	Practical Task	Tools Used	Learning Outcome
1	Implement SR, JK, D, and T Flip-Flops using logic gates	Digital Trainer Kit, Logic	Understand the working and truth tables of various

		Simulator	flip-flops
2	Design a 4-bit register using D Flip-Flops	Logic Simulator	Learn how data is stored using registers
3	Realize Serial-In Serial-Out (SISO) and Serial-In Parallel-Out (SIPO) Shift Registers	Logic Simulator	Analyze shifting operations using different modes
4	Implement a Counter using T Flip-Flops	Logic Simulator	Understand the operation of counters and count sequences
5	Design and test a mod-Counter (e.g., Mod-4/Mod-10)	Logic Simulator	Develop counters and verify sequences

Evaluation Method

Sr. No.	Evaluation Component	SEE (Marks)	CCE (Marks)	Description
1	Design a Sequential Circuit based on the application	15	–	Design a sequential circuit using flip-flops, registers, shift registers, or counters. Demonstrate circuit behavior through simulation or a trainer kit.
2	Shift Register Design	–	5	Design and verify Serial-In Serial-Out (SISO) and Serial-In Parallel-Out (SIPO) shift registers using simulation tools.
3	Counter Design and Testing	–	5	Implement counters (e.g., Mod-N) and verify correct count sequences using a simulator or trainer

				kit.		
	Total	15	10			

5	**State Machines** **Topics:** • Basics of State Machines • Difference between Mealy and Moore Machines • Drawing State Transition Diagrams • State Transition Tables • Applications of State Diagrams **Practical:**	**T:12** **P:06**	**20%**

Sr. No.	Practical Task	Tools Used	Learning Outcome
1	Construct a Mealy state machine using a state diagram	FSM Simulator (e.g., Evan Wallace's FSM Simulator)	Understand the structural behavior and output dependency of Mealy models
2	Construct a Moore state machine using a state diagram	FSM Simulator (e.g., Evan Wallace's FSM Simulator)	Learn to represent output-independent FSM using Moore model diagrams
3	Write VHDL code for a 3-state Mealy machine	VHDL Compiler / IDE	Gain experience coding FSM behavior in hardware description language
4	Write VHDL code for a 3-state Moore machine	VHDL Compiler / IDE	Understand the coding structure for Moore-type FSM
5	Simulate and verify a simple vending machine FSM	Digital Simulator / Embedded FSM Toolkits	Apply FSM logic to solve real-world sequential control problems

Evaluation Method

Sr. No.	Evaluation Component	SEE (Marks)	CCE (Marks)	Description
1	FSM Analysis and State Diagram Construction	15	–	Analyze a finite state machine and construct its state diagram and transition table. Identify whether it follows the Mealy or Moore model.
2	Concept Quiz (Multiple Choice Questions)	–	5	Quiz covering topics such as state machine types, transition logic, and real-world applications.
3	Viva Voce (Oral Assessment)	–	5	Oral evaluation based on Mealy vs Moore machines, FSM implementation in VHDL, and application-based reasoning.
	Total	15	10	

Project

Objective

This unit bridges theoretical knowledge with practical application by encouraging students to design, build, simulate, and present a real-world digital system using combinational and sequential circuits. Students will engage in problem-solving, teamwork, and documentation, simulating an industry project.

Evaluation Method

Sr. No.	Evaluation Component	SEE (Marks)	CCE (Marks)	Description
1	Report	5	-	Project documentation with design and results.
2	Presentation	5	-	A brief explanation of project work and logic.
3	Model Working	10	-	Functional and accurate circuit/model output.
4	Viva	10	-	Oral questions on design, logic, and contribution.

Suggested Specification Table with Marks:

Distribution of Marks (Revised Bloom's Taxonomy)						
Level	Remembrance (R)	Understanding (U)	Application (A)	Analyze (N)	Evaluate (E)	Create (C)
Weightage %	10%	15%	20%	10%	15%	30%

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the evaluation may vary slightly from the above table.

Course Outcome:

After learning the course, the students should be able to:	
CO1	Convert and operate on different number systems and analyze the functioning of basic and universal logic gates.

CO2	Simplify Boolean expressions using Boolean algebra and Karnaugh Maps (K-maps).
CO3	Design and simulate various combinational logic circuits, including adders, subtractors, encoders, decoders, and multiplexers.
CO4	Analyze and construct sequential circuits using flip-flops, registers, shift registers, and counters.
CO5	Represent and differentiate Mealy and Moore finite state machines (FSMs) using standard notations and implement them using state diagrams and VHDL.

Instructional Method:

The course delivery method will depend on the requirements of the content and the needs of students. The teacher, in addition to the conventional teaching method by the blackboard, may also use any of the tools such as demonstration, role play, quizzes, brainstorming, MOOCs, etc.

From the content, 10% of topics are suggested for flipped mode instruction.

Students will utilize supplementary resources, including online videos, NPTEL/SWAYAM videos, e-courses, and Virtual Laboratories.

The internal evaluation will be done on the basis of the CCE-Continuous and Comprehensive Evaluation.

SEE: Semester End Evaluation will be conducted at the end of the semester for evaluation of the performance of students in the laboratory.

Reference Books

[1] M. M. Mano, Digital Logic and Computer Design. Pearson Education, 2005.

[2] T. L. Floyd, Digital Fundamentals, 10th ed. Pearson Education, 2009.

[3] R. P. Jain, Modern Digital Electronics, 4th ed. McGraw-Hill Education, 2009.

[4] Z. Kohavi and N. K. Jha, Switching and Finite Automata Theory, 3rd ed. Cambridge, U.K.: Cambridge Univ. Press, 2010.

[5] J. F. Wakerly, Digital Design: Principles and Practices, 4th ed. Upper Saddle River, NJ, USA: Pearson Prentice Hall, 2006.

[6] C. H. Roth Jr. and L. L. Kinney, Fundamentals of Logic Design, 7th ed. Boston, MA, USA: Cengage Learning, 2013.