Gyanmanjari Innovative University

Syllabus
Gyanmanjari Institute of Technology
Semester-2 (B. Tech)

Subject: Digital Electronics: Logic Design and Circuit Implementation – BET1EE12302

Type of course: Engineering Science Courses

Prerequisite: Basic knowledge of Physics and Mathematics.

Rationale:

The course is designed to introduce the fundamental concepts of Digital Electronics to engineering students. Digital electronics forms the backbone of modern computing and digital systems and is integral to technologies such as computers, communication networks, embedded systems, automation, and consumer electronics. A strong foundation in digital electronics is essential for students and professionals to design, analyze, and develop reliable digital systems in the 21st-century technological landscape. Without digital electronics, a modern information-driven society would not be possible.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks		Total Marks
CI	T	P	C	SEE	CCE	
2	0	4	4	100	50	150

Legends: CI-Classroom Instructions; T-Tutorial; P -Practical; C –Credit; ESE -End Semester Examination; MSE-Mid Semester Examination; V–Viva; CA-Continuous Assessment; ALA-Active Learning Activities.

Course Content:

Sr. No.	Course Content	Hrs.	% Weightage
1	**Fundamentals of Digital Electronics and Logic Design** ***Theory Topics:*** Fundamentals of Digital Systems covering digital versus analog systems, advantages of digital systems, number systems and their conversions, binary arithmetic, basic and universal logic gates, Boolean algebra, De Morgan's theorems, and Boolean functions. ***Practical:*** 1. Practical demonstration of analog vs digital signals using CRO/DSO and a signal generator. 2. Study and verification of basic logic gates	15	25 %

3. Study and verification of universal logic gates: NAND (7400) and NOR (7402)
4. Implementation of basic gates using NAND gates only
5. Implementation of basic gates using NOR gates only
6. Study and verification of Exclusive-OR (XOR) and Exclusive-NOR (XNOR) gates
7. Verification of De Morgan's Theorems

Evaluation Method:

Sr. No.	Evaluation Method	SEE (Marks)	CCE (Marks)
1.	**Problem Solving on Number System:** Solve the problem of number system conversion: Solve the problem of number system conversion	10	–
2.	**Circuit Design Ability of Boolean function using Gates:** Ability to design digital circuits as per given specifications (logic gates)	05	–
3.	**Logic Implementation & Verification:** Verification of truth tables, Boolean expressions:	05	–
4.	**Active Learning Activity (validate the Boolean function using a truth table):** Verify the given Boolean function by constructing and analyzing its corresponding truth table	–	05
5.	**Poster Presentation:** Study the operation of basic flip-flops (SR, JK, D, and T) and analyze their output responses for different input and clock conditions.	–	05
	Total	20	10

2	**Combinational Logic Circuits and Karnaugh Map Simplification** ***Theory Topics:*** Introduction to combinational digital circuits covering SOP and POS representations, implementation using universal gates, and logic minimization using Karnaugh maps with don't-care conditions. ***Practical:***	08	10%

1. Implementation of SOP Boolean expressions derived from truth tables using logic gates.
2. Implementation of POS Boolean expressions using universal gates (NAND / NOR).
3. Simplification of Boolean expressions using 2, 3, and 4-variable Karnaugh maps.
4. Simplification of Boolean functions using Karnaugh maps with don't-care conditions.

Evaluation Method:

Sr. No.	Evaluation Methods	SEE	CCE
1	**Simplify Boolean functions using SOP & POS and verify using any software:** Numerical based on Simplify Boolean functions.	10	
2	**Active Learning Assignment (K-Map):** Numerical based on simplified Boolean functions	10	
3	**Validate Boolean functions using truth tables and simulation:** analyze the given Boolean expressions or logic circuits, judge the correctness of the logical approach, and draw the appropriate logic diagram.		10
	Total	20	10

3	**Combinational Building Blocks**	10	20%

Theory Topics:

Multiplexers, Demultiplexers, Encoders, Decoders, code converters, Comparators, Adders, and parity-based error control circuits.

Practical:

1. Design and implementation of multiplexer circuits (2:1 and 4:1) using logic gates.
2. Design and implementation of demultiplexer circuits.
3. Design and verification of encoder, decoder, and priority encoder circuits.
4. Design and implementation of binary adder and adder–subtractor circuits using logic gates.
5. Design and implementation of a digital comparator for magnitude comparison.
6. Design and verification of parity generator and parity checker.

circuits.

7. Design and implementation of code converters (Binary-to-Gray, Gray-to-Binary, BCD-to-Binary).
8. Design and implementation of a carry-look-ahead adder and comparison with a ripple-carry adder.

Evaluation Method:

Sr. No.	Evaluation Methods	SEE	CCE
1	**Designing a circuit in a software tool & finding the output characteristics:** Simulation Half Adder & Full Adder circuit Design in a software tool	10	
2	**Judge and Draw:** Predict outputs for a given logic problem and draw the corresponding circuit. Students will be able to analyze a logic problem and design an appropriate combinational circuit		10
	Total	10	10

4	**Sequential Circuits (Flip-Flops, Registers & Counters)**	12	20%

Theory Topics:

Sequential circuits and systems, including differences between combinational and sequential circuits, memory elements, latches, and clocked flip-flops. Registers and shift registers, including bidirectional and universal shift registers, as well as counters such as modulo-n, synchronous, and asynchronous counters, along with their applications.

Practical:

1. Design and implement an SR flip-flop and observe the toggle operation. Students will be able to analyze and implement SR flip-flops.
2. Design and implement a J-K flip-flop and observe toggle operation. Students will be able to analyze and implement J-K flip-flops.
3. Design and implement T and D flip-flops using logic gates or ICs. Students will be able to analyze and implement J-K flip-flops.
4. Design and implement bi-directional shift registers. Students will be able to analyze data shifting in both directions. waveform over time.
5. Design and implement a modulo-n counter. Students will be able to design synchronous counting circuits.
6. Design and implement a Johnson counter. Students will be able to analyze and implement Johnson counters.
7. Design and implement a ripple UP counter. Students will be able to analyze propagation delay in ripple counters.

8. Design and implement a ripple-down counter. Students will be able to design and verify down-counting circuits.

Evaluation Method:

Sr. No.	Evaluation Methods	SEE	CCE
1	**Design and simulate a counter for the specified function using Multisim:** Students research, design, simulate, and then build and test their circuits. and explain their results.	10	
2	**Analyze the behavior of flip-flops and observe the respective circuit outputs.** Analyze the operating characteristics of various flip-flops and verify their output responses through circuit simulation.	10	
3	**Quiz (MCQ – Conceptual & Circuit-based)** Analysis of flip-flops, MCQ-based quizzes, and questions on flip-flops, multiplexers, and demultiplexers to strengthen conceptual and circuit-level understanding	–	05
4	**Circuit Demonstration**: Students demonstrate their designed circuits to the instructor, showing correct operation and explaining the working principle.		05
	Total	20	10

5	**State Machine Analysis and Design** ***Theory Topics:*** Introduction to sequential circuits, concept of states and state transitions, state diagrams and state tables, Mealy and Moore state machines, state equations and output equations, state reduction techniques, sequence detectors, implementation of state machines using flip-flops, and basic timing considerations. ***Practical:*** 1. Design and simulation of a Moore Finite State Machine using D flip-flops in Multisim. 2. Design and simulation of a Mealy Finite State Machine using JK flip-flops in Multisim. 3. Construction and simulation of state diagrams and state tables for given FSM specifications. 4. State reduction and state assignment, followed by FSM implementation and simulation.	15	25 %

5. Design and simulation of a sequence detector using the FSM approach.
6. Timing analysis and verification of FSM operation using timing diagrams
7. Design and simulation of an application-based FSM (Traffic Light Controller / Vending Machine).
8. Observation and analysis of propagation delay and clock effects in sequential circuits.

Evaluation Method:

Sr. No.	Evaluation Methods	SEE	CCE
1	Timing Diagram Verification evaluates propagation delay, clock effects, and proper sequencing in sequential circuits.	10	
2	Troubleshooting Exercises: Students are given faulty circuits and must diagnose and correct errors to demonstrate practical problem-solving skills.		5
3	Observation of Propagation Delay: Students verify and understand timing effects on sequential circuits.		5
	Total	10	10

Project

Objective

This unit bridges theoretical knowledge with practical application by encouraging students to design, build, simulate, and present a real-world digital system using combinational and sequential circuits. Students will engage in problem-solving, teamwork, and documentation, simulating an industry project.

Evaluation Method

Sr. No.	Evaluation Component	SEE (Marks)	CCE (Marks)
1	**Report** Project documentation with design and results.	5	-
2	**Presentation** A brief explanation of the project work and logic.	5	-
3	**Model Working** Functional and accurate circuit/model output.	5	-

	4	**Viva** Oral questions on design, logic, and contribution.	5	-			
		Total	20	-			

Suggested Specification table with Marks (Theory): 100

Distribution of Marks **(Revised Bloom's Taxonomy)**						
Level	Remembrance (R)	Understanding (U)	Application (A)	Analyze (N)	Evaluate (E)	Create (C)
Weightage %	10%	15%	20%	10%	15%	30%

Course Outcome:

After learning the course, the students should be able to:	
CO1	Understand number systems, logic gates, and Boolean algebra for digital system analysis.
CO2	Design and simplify combinational logic circuits using SOP, POS, and Karnaugh maps.
CO3	Implement and analyze combinational building blocks such as multiplexers, decoders, adders, and comparators.
CO4	Design and analyze sequential circuits including flip-flops, registers, and counters.
CO5	Model, design, and implement finite state machines for real-world digital applications.

Instructional Method:

The course delivery method will depend on the requirements of the content and the needs of students. The teacher, in addition to the conventional teaching method by the blackboard, may also use any of the tools, such as demonstration, role play, quizzes, brainstorming, MOOCs, etc.

From the content, 10% of topics are suggested for flipped-mode instruction.

Students will utilize supplementary resources, including online videos, NPTEL/SWAYAM videos, e-courses, and Virtual Laboratories.

The internal evaluation will be done on the basis of the CCE-Continuous and Comprehensive Evaluation.

SEE: Semester End Evaluation will be conducted at the end of the semester for the evaluation of the performance of students in the laboratory.

Reference Books

[1] M. M. Mano, Digital Logic and Computer Design. Pearson Education, 2005.

[2] T. L. Floyd, Digital Fundamentals, 10th ed. Pearson Education, 2009.

[3] R. P. Jain, Modern Digital Electronics, 4th ed. McGraw-Hill Education, 2009.

[4] Z. Kohavi and N. K. Jha, Switching and Finite Automata Theory, 3rd ed. Cambridge, U.K.: Cambridge Univ. Press, 2010.