Gyanmanjari Innovative University

Course Syllabus
Gyanmanjari Diploma Engineering College
Semester–5

Subject: VLSI Design - DETEC15211

Type of course: Major

Prerequisite: Basic Electronics, Fundamentals of Programming

Rationale:
This course requires students to have a fundamental understanding of electronics and digital systems. Prior knowledge of semiconductor devices, basic circuit theory, and digital logic design is essential. Understanding hardware description languages (HDL) like Verilog or VHDL, will support effective learning. Basic programming skills and familiarity with simulation tools are recommended.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks					Total Marks
				Theory Marks		Practical Marks		CA	
CI	T	P	C	ESE	MSE	V	P	ALA	
4	0	2	5	60	30	10	20	30	150

Legends: CI-Class Room Instructions; T – Tutorial; P - Practical;C – Credit;ESE - End SemesterExamination; MSE- Mid Semester Examination; V – Viva; CA - Continuous Assessment;

Course Content:

Unit. No	Course content	Hrs	% Weightage
1	**Introduction to VLSI and MOS Transistor** VLSI basics, Types of VLSI design, advantages, disadvantages, applications of VLSI, digital system VLSI design, VLSI MOS structure - MOSFET transistor, MOSFET working, MOSFET current- voltage Characteristics	12	20%
2	**MOS Inverters** MOS Inverter : concept and working, Resistive load Inverter, Inverter with n-type MOSFET Load, Enhancement load NMOS, Depletion Load NMOS, CMOS Inverter: Circuit operation and description.	12	20%

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3	**MOS Circuits** Combinational Logic Circuits - two input NAND and NOR Gate with depletion NMOS load, Sequential MOS circuit SR latch NOR and NAND gate circuit, clocked SR latch, clocked JK Flip-Flop, clocked D Flip- Flop.	12	20%
4	**Fabrication of MOSFET** VLSI design flow, Y chart, Define terms: hierarchy, regularity, modularity, locality, Lithography, Etching, Deposition, Oxidation, Ion implantation, Diffusion.	12	20%
5	**VHDL Basics** Module definition and Describing design, Logic gate implementation in VHDL, VHDL for adder and subtractor circuits, Combinational circuits : Multiplexer , Demultiplexer, Decoder and Encoder, Basic Sequential circuits : SR latch, D F/F, T F/F, JK F/F.	12	20%

Continuous Assessment:

Sr. No	Active Learning Activities	Marks
1	**Case Study:** The students will individually analyze the Case Study on Real-World VLSI Applications (e.g., microprocessors, mobile chip, digital watch) and upload a report on GMIU web portal.	10
2	**Verilog Coding & Simulation:** Students have to Design and Simulate using Verilog code for combinational and sequential circuits and upload the result of simulation on GMIU web portal.	10
3	**Design Task:**Students will individually draw and explain any applications design Circuits using Mos fabrication, For example : Draw CMOS diagram (PMOS + NMOS) and explain how it works (no software needed) and upload pdf on GMIU web portal.	10
Total		**30**

Suggested Specification table with Marks (Theory): NA

Distribution of Theory Marks (Revised Bloom's Taxonomy)						
Level	Remembrance (R)	Understanding (U)	Application (A)	Analyze (N)	Evaluate (E)	Create (C)
Weightage	20%	30%	30%	10%	5%	5%

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

Course Outcomes:

After learning the course the students should be able to:	
CO1	Understand the fundamentals of MOS technology and analyze the operation of MOS inverters.
CO2	Analyze and design basic MOS circuits using CMOS logic principles.
CO3	Evaluate the performance of MOS circuits in terms of power, delay, and scaling effects.
CO4	Interpret the fabrication process of MOSFETs and its impact on device characteristics.
CO5	Apply the basics of hardware description using VHDL for simple digital circuit design and simulation.

List of Practicals :

Sr. No.	Descriptions	Unit. No	Hrs
1	To study of MOSFET current- voltage Characteristics,	1	2
2	To study of Enhancement load NMOS, Depletion Load NMOS	2	2
3	Simulate the Basic logic gates using VHDL.	3,5	2
4	Simulate universal gates using VHDL	3,5	2
5	Simulate XOR and XNOR using VHDL	3,5	2
6	Simulate Half adder using VHDL	3,5	2
7	Simulate full adder using half adder in VHDL	3,5	2
8	Simulate 4 x1 multiplexer using VHDL	3,5	2
9	Simulate 1 x 4 de-mux using VHDL	3,5	2
10	Simulate 3 : 8 decoder using VHDL	3,5	2
11	Simulate 8 : 3 encoder using VHDL	3,5	2
12	Simulate flip-flops (SR , D, T, JK) using VHDL	3,5	2
13	Simulate 4 bit Up counter using VHDL	3,5	2
14	Simulate 4 bit shift register using VHDL	3,5	2

15	To study of fabrication techniques : Lithography and Etching,	4	**2**
	Total		**30**

Instructional Method:

The course delivery method will depend upon the requirement of content and the needs of students. The teacher, in addition to conventional teaching methods by black board, may also use any tools such as demonstration, role play, Quiz, brainstorming, MOOCs etc.

From the content 10% topics are suggested for flipped mode instruction.

Students will use supplementary resources such as online videos, NPTEL/SWAYAM videos, e-courses, Virtual Laboratory.

The internal evaluation will be done on the basis of Active Learning Assignment.

Practical/Viva examination will be conducted at the end of semester for evaluation of performance of students in the laboratory.

Reference Books:

[1] N. H. E. Weste and D. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th ed. Boston, MA, USA: Addison-Wesley, 2011.

[2] C. Mead and L. Conway, Introduction to VLSI Systems. Reading, MA, USA: Addison-Wesley, 1980.

[3] S. Brown and Z. Vranesic, Fundamentals of Digital Logic with VHDL Design, 3rd ed. New York, NY, USA: McGraw-Hill Education, 2009.

[4] M. M. Mano and M. D. Ciletti, Digital Design with an Introduction to the Verilog HDL, 5th ed. Upper Saddle River, NJ, USA: Pearson Education, 2013.

[5] S. Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, 2nd ed. Upper Saddle River, NJ, USA: Prentice Hall, 2003