Gyanmanjari Innovative University

Syllabus
Gyanmanjari Diploma Engineering College
Semester-1 (Diploma)

Subject: Building Blocks of Digital Systems - DET2EE11201

Type of course: Engineering Science Courses

Prerequisite: Basic understanding of electrical components, circuit fundamentals, logical reasoning, and elementary mathematics.

Rationale: This course introduces the fundamental concepts of digital systems, including number systems, logic gates, Boolean algebra, combinational and sequential circuits, and digital system design. It develops the knowledge and practical skills required to analyze, design, simulate, and implement basic digital circuits using standard ICs and simulation tools. The course provides a strong foundation for advanced studies in digital electronics, microprocessors, embedded systems, communication systems, and automation while preparing students for real-world engineering applications through project-based and activity-oriented learning.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks		Total Marks
CI	T	P	C	SEE	CCE	
4	0	2	5	100	50	150

Legends: CI-Class Room Instructions; T – Tutorial; P - Practical; C – Credit; SEE - Semester End Evaluation; LWA - Lab Work Assessment; V – Viva voce; CCE-Continuous and Comprehensive Evaluation; ALA- Active Learning Activities.

Course Content:

Sr. No	Course Content	Hrs.	% Weightage
1	**Number Systems and Logic Gates** • Introduction to Digital Systems and Number Systems. • Decimal, Binary, Octal, and Hexadecimal Number Systems. • Number System Conversions (Decimal, Binary, Octal, Hexadecimal). • Binary Arithmetic: Binary Addition and Subtraction. • 1's Complement and 2's Complement Representation. • Introduction to Logic Gates. • Basic Logic Gates: AND, OR, NOT. • Universal Gates: NAND and NOR.	18	20%

- Exclusive Gates: XOR and XNOR.
- Truth Tables, Logic Symbols, and Logic Expressions.
- Realization of Basic Gates using Universal Gates.
- Applications of Logic Gates in Digital Systems.

Practical:

1. To perform decimal-to-binary, binary-to-decimal, octal, and hexadecimal conversions.
2. To perform binary addition and subtraction using binary numbers.
3. To perform 1's complement and 2's complement operations.
4. To verify the truth tables of basic logic gates (AND, OR, NOT) using a Digital Trainer Kit or simulation software.
5. To implement NAND, NOR, XOR, and XNOR gates and verify their truth tables.
6. To realize AND, OR, and NOT gates using only NAND gates.
7. To realize AND, OR, and NOT gates using only NOR gates.
8. To verify universal gate realization using the Digital Trainer Kit.
9. To design and simulate simple logic circuits using basic logic gates.
10. To implement a simple real-life digital application (such as automatic lamp control, alarm circuit, or voting logic) using logic gates on a breadboard or simulator.

Evaluation Method

Sr. No.	Evaluation Component	SEE (Marks)	CCE (Marks)
1	Number System Conversion and Binary Arithmetic	10	–
2	Digital Logic Circuit Implementation	10	–
3	Logic Gate Application and Real-life Logic Design (ALA-1)	–	10
	Total	**20**	**10**

Examination Style

Number System Conversion and Binary Arithmetic (10 Marks)

	Students will solve problems related to number system conversions between Decimal, Binary, Octal, and Hexadecimal systems. They will also perform binary addition, subtraction, 1's complement, and 2's complement operations. Students should apply appropriate conversion methods and arithmetic rules while presenting systematic calculations. Marks will be awarded based on correctness of conversions, binary operations, logical approach, and presentation. **Digital Logic Circuit Implementation (10 Marks)** Students will implement the given logic circuit using basic logic gates or universal gates (NAND/NOR) on a Digital Trainer Kit or simulation software. They will generate the truth table, verify the logical operation, and explain the working of the implemented circuit. Marks will be awarded based on circuit implementation, correctness of truth table, logical verification, and interpretation of results. **Logic Gate Application and Real-life Logic Design (ALA-1) (10 Marks)** Students will identify a real-life application of digital logic (such as automatic lighting, security alarm, water level indicator, or voting system), design the corresponding logic circuit using logic gates, simulate or implement the circuit, and upload the report with screenshots and explanation on the GMIU Web Portal. Marks will be awarded based on originality of the application, correctness of logic design, implementation, technical explanation, and report quality.		
2	**Boolean Algebra and Logic Simplification** ***Theory Topics:*** • Introduction to Boolean Algebra. • Boolean Variables and Boolean Functions. • Basic Boolean Laws and Theorems. • De Morgan's Theorems. • Simplification of Boolean Expressions. • Canonical Forms: Sum of Products (SOP), Product of Sums (POS) • Minterms and Maxterms. • Karnaugh Maps (K-Maps): 2-variable, 3-variable. • Realization of Simplified Boolean Expressions using Basic and Universal Gates. • Applications of Boolean Algebra in Digital Circuit Design.	**18**	**20%**

Practical:

11. To verify Boolean laws and De Morgan's Theorems using the Digital Trainer Kit or simulation software.
12. To simplify Boolean expressions using Boolean Algebra.
13. To simplify 2-variable Boolean expressions using Karnaugh Maps.
14. To simplify 3-variable Boolean expressions using Karnaugh Maps.
15. To simplify 4-variable Boolean expressions using Karnaugh Maps.
16. To realize simplified Boolean expressions using basic logic gates.
17. To implement SOP expressions using NAND gates only.
18. To implement POS expressions using NOR gates only.
19. To simulate and verify Boolean expressions using Logisim or Multisim.
20. To design and implement a real-life digital logic circuit using Boolean simplification techniques.

Evaluation Method

Sr. No.	Evaluation Component	SEE (Marks)	CCE (Marks)
1	Boolean Expression Simplification using K-Map	10	–
2	Logic Circuit Design and Implementation	10	–
3	SOP/POS Conversion and Logic Verification (ALA-2)	–	10
	Total	**20**	**10**

Examination Style

Boolean Expression Simplification using K-Map (10 Marks)

Students will simplify the given Boolean expression using Boolean algebra and Karnaugh Maps (2, 3, or 4 variables). They should obtain the minimum expression and verify the correctness using truth tables. Marks will be awarded based on the correctness of grouping, simplification, verification, and presentation.

	Logic Circuit Design and Implementation (10 Marks) Students will implement the simplified Boolean expression using basic logic gates or universal gates (NAND/NOR) using Digital Trainer Kit or simulation software. They will verify the truth table and explain the circuit operation. Marks will be awarded based on correct implementation, verification, understanding of logic realization, and interpretation of results. **SOP/POS Conversion and Logic Verification (ALA-2) (10 Marks)** Students will convert the given Boolean expression from SOP to POS or POS to SOP form. They will verify both expressions using simulation software or truth tables and submit the implementation report with screenshots on the GMIU Web Portal. Marks will be awarded based on correctness of conversion, verification, simulation results, technical explanation, and report quality.		
3	**Combinational Logic Circuits** ***Theory Topics:*** • Introduction to Combinational Logic Circuits. • Half Adder and Full Adder. • Half Subtractor and Full Subtractor. • Multiplexers (MUX) and Demultiplexers (DEMUX). • Design and Implementation of Combinational Logic Circuits using Standard ICs and Simulation Software. ***Practical:*** 21. To design and implement a Half Adder using logic gates and verify its truth table. 22. To design and implement a Full Adder using logic gates and verify its truth table. 23. To design and implement a Half Subtractor and Full Subtractor. 24. To implement a 4-bit Parallel Binary Adder using ICs or simulation software. 25. To implement and verify Encoder and Decoder circuits using Digital Trainer Kit or ICs. 26. To implement a 4-to-1 Multiplexer and 1-to-4 Demultiplexer using ICs or simulation software. 27. To design a Magnitude Comparator and verify its operation. 28. To design and simulate a real-life combinational logic application (traffic light selection, digital lock, alarm selector, voting logic, etc.) using combinational circuits.	**27**	**30%**

Evaluation Method

Sr. No.	Evaluation Component	SEE (Marks)	CCE (Marks)
1	Combinational Circuit Design and Analysis	10	–
2	Code Converter / MUX-DEMUX Implementation	10	–
3	Design of a Real-Life Combinational Logic Application (ALA-3)	–	10
	Total	**20**	**10**

Examination Style

Combinational Circuit Design and Analysis (10 Marks)

Students will design the given combinational logic circuit such as an adder, subtractor, comparator, encoder, decoder, or multiplexer using logic gates or standard ICs. They will generate the truth table, verify the circuit operation through simulation or hardware implementation, and explain the working of the circuit. Marks will be awarded based on circuit design, correctness of implementation, logical verification, and interpretation of results.

Code Converter / MUX-DEMUX Implementation (10 Marks)

Students will implement the given code converter (Binary–Gray, Gray–Binary, BCD–Excess-3, etc.) or Multiplexer/Demultiplexer circuit using Digital Trainer Kit or simulation software. They will verify the circuit using appropriate test inputs and explain its practical applications. Marks will be awarded based on implementation accuracy, verification, circuit analysis, and presentation.

Design of a Real-Life Combinational Logic Application (ALA-3) (10 Marks)

Students will design and implement a real-life combinational logic application such as a digital voting system, automatic alarm system, security access logic, traffic signal selector, or industrial control logic using simulation software or hardware. Students shall submit the circuit diagram, simulation screenshots, observations, and a brief report on the GMIU Web Portal. Marks will be awarded based on originality,

	correctness of logic design, implementation, technical explanation, and report quality.		
4	**Sequential Logic Circuits** *Theory Topics:* • Introduction to Sequential Logic Circuits. • Difference between Combinational and Sequential Circuits. • Latches and Flip-Flops. • SR Flip-Flop. • JK Flip-Flop. • D Flip-Flop. • T Flip-Flop. • Registers and Types of Registers. • Shift Registers • Counters • Applications of Sequential Logic Circuits in Digital Systems. *Practical:* 29. To implement and verify the truth tables of SR, JK, D, and T Flip-Flops using Digital Trainer Kit or simulation software. 30. To design and implement a 4-bit register using D Flip-Flops. 31. To implement and verify a Serial-In Serial-Out (SISO) Shift Register. 32. To implement and verify a Serial-In Parallel-Out (SIPO) Shift Register. 33. To implement and verify a Parallel-In Serial-Out (PISO) Shift Register. 34. To implement and verify a Parallel-In Parallel-Out (PIPO) Shift Register. 35. To design and implement a 4-bit Ripple Counter. 36. To design and implement a Synchronous Up Counter. 37. To design and implement a Mod-10 (Decade) Counter. 38. To design and simulate a sequential logic application such as a digital event counter, visitor counter, LED running sequence, or simple timing circuit. **Evaluation Method** **Sr. No.** | **Evaluation Component** | **SEE (Marks)** | **CCE (Marks)** 1 | Sequential Circuit Design and Analysis | 10 | –	**18**	**20%**

	2	Register and Counter Implementation	10	–		
	3	Sequential Logic Based Mini Application (ALA-4)	–	10		
		Total	**20**	**10**		

Examination Style

Sequential Circuit Design and Analysis (10 Marks)

Students will design and implement the given sequential logic circuit using flip-flops, registers, or shift registers using Digital Trainer Kit or simulation software. They will verify the circuit operation using timing diagrams or output observations and explain the working principle. Marks will be awarded based on correct circuit implementation, verification, analysis, and interpretation of results.

Register and Counter Implementation (10 Marks)

Students will implement the assigned register or counter circuit such as SISO, SIPO, PISO, PIPO, Ripple Counter, Synchronous Counter, or Mod-N Counter using simulation software or hardware. Students should verify the output sequence and explain the operation and practical applications of the circuit. Marks will be awarded based on implementation accuracy, output verification, circuit analysis, and presentation.

Sequential Logic Based Mini Application (ALA-4) (10 Marks)

Students will design and implement a simple sequential logic application such as a digital visitor counter, event counter, LED running sequence, traffic signal timer, or digital timer using flip-flops, registers, or counters. Students shall submit the circuit diagram, simulation screenshots, observations, and a brief report on the GMIU Web Portal. Marks will be awarded based on originality, correctness of circuit design, implementation, technical explanation, and report quality.

5	**Digital System Design and Applications** ***Theory Topics:*** • Introduction to Digital System Design. • Digital Integrated Circuits (ICs) • Design Methodology for Digital Systems.	**09**	**10%**

- Hardware Implementation using Digital Trainer Kit and Breadboard.
- Simulation of Digital Circuits using Logisim/Multisim.
- Troubleshooting Digital Circuits.
- Testing and Verification of Digital Systems.
- Applications of Digital Systems
- Introduction to Mini Project Development and Documentation.

Practical:

39. To identify and verify the pin configuration and operation of commonly used digital ICs (7400, 7402, 7404, 7408, 7432, 7486, etc.).
40. To implement a digital circuit using standard TTL/CMOS ICs on a breadboard.
41. To simulate a digital system using Logisim or Multisim and verify its operation.
42. To troubleshoot and rectify faults in a given digital logic circuit.
43. To design and implement a Digital Voting Machine.
44. To design and implement a Password-Based Digital Lock using logic gates.
45. To design and implement a Water Tank Level Indicator using digital logic.
46. To design and implement an Automatic Street Light Controller using digital logic.
47. To develop a mini digital system by integrating combinational and sequential circuits.
48. To demonstrate, test, and document the mini project with circuit diagram, simulation results, hardware implementation, and report.

Evaluation Method

Sr. No.	Evaluation Component	SEE (Marks)	CCE (Marks)
1	Digital System Design and Implementation	10	–
2	Hardware Testing, Troubleshooting and Demonstration	10	–
3	Mini Project Development and Presentation (ALA-5)	–	10
	Total	**20**	**10**

	Examination Style **Digital System Design and Implementation (10 Marks)** Students will design and implement the given digital system using logic gates, combinational circuits, sequential circuits, or standard digital ICs. The implementation may be carried out using a Digital Trainer Kit, breadboard, or simulation software. Students shall explain the design methodology, verify the circuit operation, and interpret the obtained results. Marks will be awarded based on circuit design, implementation accuracy, verification, and technical explanation. **Hardware Testing, Troubleshooting and Demonstration (10 Marks)** Students will be provided with a digital circuit containing intentional faults or incomplete connections. They are required to identify the fault, rectify the circuit, verify its operation, and demonstrate the correct working of the circuit using appropriate measuring instruments or simulation software. Marks will be awarded based on fault identification, troubleshooting skills, successful implementation, and interpretation of observations. **Mini Project Development and Presentation (ALA-5) (10 Marks)** Students will design and develop a simple digital system by integrating the concepts learned throughout the course. The project may include applications such as a digital voting machine, automatic lighting system, water level indicator, password lock, digital counter, or similar digital application. Students shall submit the circuit diagram, simulation results, hardware implementation photographs, observations, and project report, followed by a presentation on the GMIU Web Portal. Marks will be awarded based on originality, design methodology, implementation, technical understanding, documentation, and presentation.		

Suggested Specification Table with Marks:

Distribution of Marks (Revised Bloom's Taxonomy)						
Level	Remembrance (R)	Understanding (U)	Application (A)	Analyze (N)	Evaluate (E)	Create (C)
Weightage %	10%	15%	20%	10%	15%	30%

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the evaluation may vary slightly from the above table.

Course Outcome:

After learning the course, the students should be able to:	
CO1	Apply number system conversions, binary arithmetic, and explain the operation of basic and universal logic gates.
CO2	Simplify Boolean expressions using Boolean algebra, De Morgan's theorems, and Karnaugh Maps (K-Maps).
CO3	Design, analyze, and implement combinational logic circuits such as adders, subtractors, encoders, decoders, multiplexers, and code converters.
CO4	Design and implement sequential logic circuits using flip-flops, registers, shift registers, and counters.
CO5	Develop, simulate, test, and troubleshoot basic digital systems using standard ICs, simulation tools, and hardware implementation techniques.

Instructional Method:

The course delivery method will depend on the requirements of the content and the needs of students. The teacher, in addition to the conventional teaching method using the blackboard, may also use any of the tools such as demonstration, role play, quizzes, brainstorming, MOOCs, etc.

From the content, 10% of topics are suggested for flipped mode instruction.

Students will utilize supplementary resources, including online videos, NPTEL/SWAYAM videos, e-courses, and Virtual Laboratories.

The internal evaluation will be done based on the CCE (Continuous and Comprehensive Evaluation).

SEE: Semester End Evaluation will be conducted at the end of the semester for the evaluation of the performance of students in the laboratory.

Reference Books

[1] M. M. Mano, Digital Logic and Computer Design. Pearson Education, 2005.

[2] T. L. Floyd, Digital Fundamentals, 10th ed. Pearson Education, 2009.

[3] R. P. Jain, Modern Digital Electronics, 4th ed. McGraw-Hill Education, 2009.

[4] Z. Kohavi and N. K. Jha, Switching and Finite Automata Theory, 3rd ed. Cambridge, U.K.: Cambridge Univ. Press, 2010.

[5] J. F. Wakerly, Digital Design: Principles and Practices, 4th ed. Upper Saddle River, NJ, USA: Pearson Prentice Hall, 2006.